

# 《集成电路与系统设计、功率与定时健

## 图书基本信息

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## 内容概要

This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2006, held in Montpellier, France, in September 2006. The 41 revised full papers and 23 revised poster papers presented together with 4 key notes and 3 industrial abstracts were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on high-level design, power estimation and modeling memory and register files, low-power digital circuits, busses and interconnects, low-power techniques, applications and SoC design, modeling, digital circuits, and reconfigurable and programmable devices.

## 书籍目录

Session 1 High-Level Design Design of Parallel Implementations by Means of Abstract Dynamic Critical Path Based Profiling of Complex Sequential Algorithms Software Simultaneous Multi-Threading, a Technique to Exploit Task- Level Parallelism to Improve Instruction- and Data-Level Parallelism Handheld System Energy Reduction by OS-Driven RefreshSession 2 Power Estimation / Modeling Delay Constrained Register Transfer Level Dynamic Power Estimation Circuit Design Style for Energy Efficiency: LSDL and Compound Domino Accurate PTV, State, and ABB Aware RTL Blackbox Modeling of Subthreshold, Gate, and PN-Junction Leakage Leakage Power Characterization Considering Process VariationsSession 3 Memory and Register Files Heuristic for Two-Level Cache Hierarchy Exploration Considering Energy Consumption and Performance System Level Multi-bank Main Memory Configuration for Energy Reduction SRAM CP: A Charge Recycling Design Schema for SRAM Compiler-Driven Leakage Energy Reduction in Banked Register FilesSession 4 Low-Power Digital Circuits Impact of Array Data Flow Analysis on the Design of Energy-Efficient Circuits Methodology for Energy-Efficient Digital Circuit Sizing: Important Issues and Design Limitations Low-Power Adaptive Bias Amplifier for a Large Supply-Range Linear Voltage Regulator Circuit Sizing and Supply-Voltage Selection for Low-Power Digital Circuit DesignSession 5 Busses and Interconnects Power Modeling of a NoC Based Design for High Speed Telecommunication Systems Partial Bus-Invert Bus Encoding Schemes for Low-Power DSP Systems Considering Inter-wire Capacitance Estimation of Power Reduction by On-Chip Transmission Line for 45nm Technology Two Efficient Synchronous—Asynchronous Converters Well-Suited for Network on Chip in GALS ArchitecturesSession 6 Low Power TechniquesSession 7 Applications and SoC DesignSession 8 ModelingSession 9 Digital CircuitsSession 10 Reconfigurable and Programmable DevicesPoster 1Poster 2Poster 3KeynotesIndustrial SessionAuthor Index

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