《Integrated Circuit a》

图书基本信息

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内容概要

This book constitutes the refereed proceedings of the 15th International Workshop on Power and Timing Optimization and Simulation, PATMOS 2005, held in Leuven, Belgium in September 2005. The 74 revised full papers presented were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on low-power processors, code optimization for low-power, high-level design, telecommunications and signal processing, low-power circuits, system-on-chip design, busses and interconnections, modeling, design automation, low-power techniques, memory and register files, applications, digital circuits, and analog and physical design.

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